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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number	10/805,720
Filing Date	03-22-2004
First Named Inventor	Li
Art Unit	2823
Examiner Name	KIM, Su C.
Attorney Docket Number	2004 P 50201 US

Sheet	1	of	2
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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
SK	1	US-5,108,935	04-28-1992	Rodder	
	2	US-5,578,228	11-18-1998	Hwang	
	3	US-5,596,218	01-21-1997	Soleimani, et al.	
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	5	US-5,714,788	02-03-1998	Ngaoaram	
	6	US-5,872,387	02-18-1999	Lyding, et al.	
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	8	US-6,051,865	04-18-2000	Gardner, et al.	
	9	US-6,100,558	08-08-2000	Krivokapic, et al.	
	10	US-6,110,784	08-29-2000	Gardner, et al.	
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	13	US-6,403,976 B1	06-11-2002	Saitoh, et al.	
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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
SK	23	EP 0 921 575 A2	06-09-1999	Matsushita Electrical Industrial Co., Ltd.		
SK	24	EP 1 020 898 A2	07-19-2000	Matsushita Electrical Industrial Co., Ltd.		

Examiner Signature		Date Considered	1/23/06
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	10/805,720
		Filing Date	03-22-2004
		First Named Inventor	Li
		Art Unit	2823
		Examiner Name	KIM, Su C.
Sheet 2 of 2	Attorney Docket Number	2004 P 50201 US	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
SK	25	ERNST, T., et al., "A New Si:C Epitaxial Channel nMOSFET Architecture with Improved Drivability and Short-Channel Characteristics," 2003, 2003 Symposium on VLSI Technology Digest of Technical Papers, 2 pages, Document No. 4-89114-035-6/03.	
SK	26	INUMIYA, S., et al., "Fabrication of HfSiON Gate Dielectrics by Plasma Oxidation and Nitridation, Optimized for 65nm node Low Power CMOS Applications," 2003 Symposium on VLSI Technology Digest of Technical Papers, 2 pages, Document No. 4-89114-035-6/03.	
SK	27	QUINONES, E., et al., "Enhanced Mobility PMOSFET's Using Tensile-Strained Si _{1-y} C _y Layers," IEEE Electron Device Letters, July 1999, pp. 338-340, Vol. 20, No. 7, IEEE.	
SK	28	WOLF, S., et al., "Silicon Processing for the VLSI Era: Vol. 1 - Process Technology," 2nd Ed., pp. 336-339, Lattice Press, Sunset Beach, CA, 2000.	

Examiner Signature		Date Considered	1/23/06
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